# CANTURK ISCI

CONTACT INFORMATION Department of Electrical Engineering

Princeton University *E-mail:* canturk@alumni.princeton.edu
Princeton, NJ 08544 USA *Web:* http://www.princeton.edu/~canturk

Phone: +1 609 468 7744

RESEARCH INTERESTS Computer architecture and its interaction with systems software

Adaptive, reliable, power-efficient and secure computing systems

**EDUCATION** 

*Ph.D.* **Princeton University**, Princeton, NJ

Sep 2001 – Jun 2007

**M.A.** Electrical Engineering

Advisor: Margaret Martonosi

M.Sc. University of Westminster, London, UK

Sep 2000 – Sep 2001

VLSI System Design (Graduated with Distinction)

Advisors: Izzet Kale and R.C.S. Morling

**B.Sc. Bilkent University**, Ankara, Turkey

Sep 1996 – Jun 2000

Electrical and Electronics Engineering (Graduated with High Honors)

Professional Experience

#### VMware Inc., Palo Alto, CA

Senior Member of Technical Staff in R&D Performance Group

Jul 2007 - Present

- Worked on performance characterization and improvement of Virtual Center Infrastructure.
- Developed a cluster-level power-performance analysis framework for Distributed Resource Scheduling and Distributed Power Management.
- Evaluated the scalability trends and the potential improvements in virtualized platforms.

## Princeton University, Department of Electrical Engineering, Princeton, NJ

Research Assistant in Parapet Research Group

Sep 2001 – Jun 2007

- Conducted research on runtime modeling of processor power and thermal behavior on real systems. Developed runtime power and temperature estimation frameworks.
- Investigated repetitive phase behavior of applications. Demonstrated effective phase classification techniques based on runtime performance monitoring and application control-flow signatures with dynamic instrumentation.
- Devised novel online phase detection, phase and duration prediction methods that are resilient to real-system variability effects for dynamically-varying application behavior.
- Designed and evaluated workload-adaptive, autonomous and predictive power management techniques for real systems and future chip multiprocessor architectures.

#### Intel Hillsboro, Corporate Technology Group/System Technology Lab, Hillsboro, OR

*Intern* in Platform Capabilities Lab

Summer 2006

Worked on energy-efficient resource allocation in heterogeneous data centers. Developed architectural feature based analytical models and training based statistical methods to predict workload behavior across platforms. Implemented a phase prediction based, workload adaptive frequency scaling governor for a new multi-core server platform. Designed allocation policies that utilize across-platform workload behavior predictors for energy-efficient management of large-scale data centers.

Managers: Ram Chary/Rick Forand, Mentor: Eugene Gorbatov

### IBM T.J. Watson Research Center, Yorktown Heights, NY

Intern in Reliability and Power Aware Microarchitectures Group

Summer 2005

Worked on global power management techniques for chip multiprocessors. Developed a trace based multiprocessor analysis tool for early evaluation of global power management policies. Explored different methods for dynamically tuning the execution of individual cores to meet chip-level power/performance goals. Designed and evaluated per-core dynamic voltage and frequency scaling policies to meet chip-wide power budget targets.

Manager: Pradip Bose, Mentor: Alper Buyuktosunoglu

#### IBM T.J. Watson Research Center, Yorktown Heights, NY

Co-op in Reliability and Power Aware Microarchitectures Group

Jul 2004 – Dec 2004

Worked on runtime performance monitoring and phase analysis of IBM POWER4 systems. Designed long-term value and duration prediction methodologies for workload performance phase behavior with applications to dynamic voltage and frequency scaling. Contributed in automated thermal microbenchmark generation for online temperature analysis of real systems. *Manager:* Pradip Bose, *Mentor:* Alper Buyuktosunoglu

# HONORS AND AWARDS

Graduate Fellowship, Princeton University, Department of Electrical Engineering 2001 – 2002
 M.Sc. with Distinction, University of Westminster, Department of Electronic 2001
 Systems, London, UK

*Millennium Scholarship*, awarded by British Council to a single candidate in Turkey 2000 – 2001 for postgraduate study in Britain

*Ranked 33<sup>rd</sup>* in National Selection Examination for Graduate Studies (LES) among approximately one hundred thousand candidates, Turkey

*Undergraduate Fellowship,* Bilkent University, Ankara, Turkey 1996 – 2000

Ranked 45th in National University Entrance Exam among approximately 1.5 million 1996 candidates, Turkey

Ranked 11th in National Physics Olympiads, Turkey

1995

#### **ACTIVITIES**

Student Member, IEEE 1999 – Present

Chair of Academic Affairs, Princeton University Graduate Student Government 2005 – 2006 Organizer of Computer Engineering Graduate Workshop (CEW), 2002 – 2003

Princeton University, Department of Electrical Engineering

Reviewer for PACT'03, HPCA'04, ISCA'04, ISLPED'04, ASPLOS'04, MICRO'04, ISLPED'05, PAC2'05, CAL'05, ISPASS'06, ASPLOS'06, SC'06, TPDS'07, TCAD'07, HPPAC'07, DAC'07, ISCA'07, TPDS'08, TACO'08

# **PUBLICATIONS**

(Electronic copies available at http://www.princeton.edu/~canturk/ETC/publications.html)

Ripal Nathuji, <u>Canturk Isci</u>, Eugene Gorbatov and Karsten Schwan, *Providing Platform Heterogeneity-Awareness for Data Center Power Management*. Under review for the Journal on Cluster Computing: Special Issue on Autonomic Computing, Sep 2007.

Ripal Nathuji, <u>Canturk Isci</u> and Eugene Gorbatov, *Exploiting Platform Heterogeneity for Power Efficient Data Centers*. In the 4th IEEE International Conference on Autonomic Computing (ICAC-2007), Jun 2007. [Acceptance rate: 13%]

<u>Canturk Isci</u>, Gilberto Contreras and Margaret Martonosi, *Live, Runtime Phase Monitoring and Prediction on Real Systems with Application to Dynamic Power Management*. In 39th ACM/IEEE International Symposium on Microarchitecture (MICRO-39), Dec 2006. [Acceptance rate: 24%]

<u>Canturk Isci</u>, Alper Buyuktosunoglu, Pradip Bose, Chen-Yong Cher and Margaret Martonosi, *An Analysis of Efficient Multi-Core Global Power Management Policies: Maximizing Performance for a Given Power Budget*. In 39th ACM/IEEE International Symposium on Microarchitecture (MICRO-39), Dec 2006. [Acceptance rate: 24%]

<u>Canturk Isci</u> and Margaret Martonosi, *Phase Detection and Prediction on Real Systems for Workload-Adaptive Power Management*. In SRC Student Symposium, Oct 2006.

<u>Canturk Isci</u> and Margaret Martonosi, *Phase Characterization for Power: Evaluating Control-Flow-Based and Event-Counter-Based Techniques*. In 12th International Symposium on High-Performance Computer Architecture (HPCA-12), Feb 2006. [Acceptance rate: 15%]

<u>Canturk Isci</u> and Margaret Martonosi, *Detecting Recurrent Phase Behavior under Real-System Variability*. In IEEE International Symposium on Workload Characterization (IISWC'05), Oct 2005. [Acceptance rate: 33%]

<u>Canturk Isci</u>, Margaret Martonosi and Alper Buyuktosunoglu, *Long-term Workload Phases: Duration Predictions and Applications to DVFS*. In IEEE MICRO, Special Issue on Energy Efficient Design, Sep/Oct 2005.

<u>Canturk Isci</u>, Zhigang Hu, Margaret Martonosi and Pradip Bose, *Building Microarchitectural Stressmarks for Thermal Testing*. In Austin Conference on Energy-Efficient Design (ACEED-2005) [*Internal Track*], Mar 2005.

<u>Canturk Isci</u>, Margaret Martonosi and Alper Buyuktosunoglu, *Workload Phase Duration Prediction and its Application to DVFS*. In Austin Conference on Energy-Efficient Design (ACEED-2005) [*Internal Track*], Mar 2005.

<u>Canturk Isci</u>, Gilberto Contreras and Margaret Martonosi, *Hardware Performance Counters for Detailed Runtime Power and Thermal Estimations: Experiences and Proposals*. In Hardware Performance Monitor Design and Functionality Workshop in conjunction with 11th International Symposium on High-Performance Computer Architecture (HPCA-11), Feb 2005.

<u>Canturk Isci</u> and Margaret Martonosi, *Runtime Power Monitoring in High-End Processors: Methodology and Empirical Data*. In 36th ACM/IEEE International Symposium on Microarchitecture (MICRO-36), Dec 2003. [Acceptance rate: 25%]

<u>Canturk Isci</u> and Margaret Martonosi, *Identifying Program Power Phase Behavior Using Power Vectors*. In 6th IEEE International Workshop on Workload Characterization (WWC-6), Nov 2003. [Acceptance rate: 30%]

# PATENTS AND DISCLOSURES

Alper Buyuktosunoglu, Pradip Bose, Chen-Yong Cher, <u>Canturk Isci</u>, Prabhakar Kudva and Margaret Martonosi, *System and Method of Efficient Resource Management by Predicting Stable Durations of a Workload Phase*. Patent filed, Jul 2006.

Eugene Gorbatov, <u>Canturk Isci</u> and Ripal Nathuji, *Method for Power-Efficient Resource Allocation in Data Centers*. Patent filed, Mar 2007.

## **THESES**

<u>Canturk Isci</u>, Workload Adaptive Power Management with Live Phase Monitoring and Prediction. Ph.D. Thesis, Princeton University, Princeton, NJ, Jun 2007.

<u>Canturk Isci</u>, *Pseudo-Random Testing of Arithmetic Circuits*. M.Sc. Thesis, University of Westminster, London, UK, Oct 2001.

# CONFERENCE PRESENTATIONS

(Electronic copies available at http://www.princeton.edu/~canturk/ETC/talks.html)

Live, Runtime Phase Monitoring and Prediction on Real Systems with Application to Dynamic Power Management, MICRO-39, Orlando, FL, Dec 2006.

An Analysis of Efficient Multi-Core Global Power Management Policies: Maximizing Performance for a Given Power Budget, MICRO-39, Orlando, FL, Dec 2006.

Phase Detection and Prediction on Real Systems for Workload-Adaptive Power Management, Semiconductor Research Corporation (SRC) Student Symposium, Cary, NC, Oct 2006.

Phase Characterization for Power: Evaluating Control-Flow-Based and Event-Counter-Based Techniques, HPCA-12, Austin, TX, Feb 2006.

Runtime Power Monitoring and Phase Analysis Methods for Power Management, SRC Annual Review in Integrated Systems Design, Columbus, OH, Feb 2006.

Detecting Recurrent Phase Behavior under Real-System Variability, IISWC'05, Austin, TX, Oct 2005.

Hardware Performance Counters for Detailed Runtime Power and Thermal Estimations: Experiences and Proposals, Performance Monitoring Workshop in HPCA-11, San Francisco, CA, Feb 2005.

Runtime Power Monitoring in High-End Processors: Methodology and Empirical Data, MICRO-36, San Diego, CA, Dec 2003.

Identifying Program Power Phase Behavior Using Power Vectors, WWC-6, Austin, TX, Nov 2003.

## **COMPUTER SKILLS**

C, Perl, Matlab, Pascal, VHDL, Verilog, Spice, Mentor Graphics EDA tools (Renoir, ModelSim, Design Architect, Leonardo, QuickFault, QuickGrade)